

## CLAIMS

We claim:

1. An emitter contact for a bipolar junction transistor comprising:  
a silicon substrate having a collector region, a base region within  
said collector region, and an emitter region within said base region;  
5 a base polysilicon layer positioned on said silicon substrate in  
contact with said base region and defining an aperture with side walls exposing  
said base and emitter regions of said silicon substrate;  
a spacer extending upwardly from said silicon substrate and  
formed to cover said side walls, said spacer covering said base region and  
10 partially covering said emitter region; and  
an emitter polysilicon layer positioned entirely within said  
aperture in engagement with said emitter region, said spacer and said substrate.
2. An emitter contact as defined in claim 1, wherein:  
said spacer defines a top edge and said emitter polysilicon defines  
a top surface; and  
said top surface of said emitter polysilicon is in alignment with  
5 said top edge of said spacer.
3. An emitter contact as defined in claim 1, wherein:  
said spacer defines a top edge and said emitter polysilicon defines  
a top surface; and  
said top surface of said emitter polysilicon is below said top edge  
5 of said spacer.
4. An emitter contact as defined in claim 1, wherein:  
said base polysilicon and said emitter polysilicon each have  
silicided top surfaces.
5. An emitter contact as defined in claim 1, wherein said emitter  
polysilicon and said base polysilicon are separated only by said spacer.

6. An emitter contact as defined in claim 1, wherein said spacer is silicon nitride.

7. An emitter contact as defined in claim 1, wherein:  
said emitter polysilicon is doped with a dopant material; and  
said emitter region is formed by the diffusion of said dopant material from said emitter polysilicon.

8. An emitter contact as defined in claim 1, wherein:  
said emitter polysilicon is laterally contained within said spacer.

9. An emitter contact as defined in claim 1, wherein said emitter polysilicon layer is 2000 to 4000 Å.

10. An emitter contact as defined in claim 1, wherein said emitter polysilicon layer is doped to a level of up to  $1E21$  atoms per cubic centimeter.

11. An emitter contact for a bipolar junction transistor comprising:  
a silicon substrate having a collector region, a base region within said collector region, and an emitter region within said base region;

5 a base polysilicon layer positioned on said silicon substrate in contact with said base region and defining an aperture with side walls exposing said base and emitter regions of said silicon substrate;

a spacer extending upwardly from said silicon substrate and formed to cover said side walls, said spacer covering said base region and partially covering said emitter region of said silicon substrate; and

10 an emitter polysilicon layer positioned in said aperture to form a plug in engagement with said emitter region and said spacer of said substrate without overlapping said base polysilicon.

12. A method for forming an emitter contact for a bipolar junction transistor comprising the steps of:

providing a silicon substrate having a collector region, a base region within said collector region, and an emitter region within said base  
5 region;

depositing a base polysilicon layer on said silicon substrate in contact with said base region, and defining an aperture with side walls exposing said base and emitter regions of said silicon substrate;

forming a spacer extending upwardly from said silicon substrate and to cover said side walls, said spacer covering said base region and partially covering said emitter region; and

forming an emitter polysilicon layer positioned within said aperture in engagement with said emitter region, said spacer and said substrate.

13. A method as defined in claim 12, wherein:

said step of depositing a base polysilicon layer further includes the steps of:

depositing a layer of oxide onto said layer of base polysilicon; and

forming said aperture through both of said layers of base polysilicon and oxide.

14. A method as defined in claim 13, wherein:

said step of forming an emitter polysilicon layer further includes the steps of:

depositing a layer of emitter polysilicon onto said oxide and into said aperture; and

etching back said layer of emitter polysilicon to stop on a top surface of said oxide layer.

15. A method as defined in claim 14, further comprising the step of etching back said layer of oxide to stop on a top surface of said base polysilicon layer.

16. A method as defined in claim 12, wherein the step of depositing the emitter polysilicon further includes the steps of:

*in situ* doping the emitter polysilicon up to a level of  $1E21$  atoms per cubic centimeter with a dopant material; and

performing a rapid thermal anneal to diffuse the dopant material.